Summer 2019 Projects

VMEC Scholar Program

Industry sites

Academic sites

2019 VMEC SUMMER SCHOLAR
BAE Systems, Inc. (Manassas, Virginia)

Company Overview:

BAE Systems plc., a global defense company, is engaged in the development, delivery, and support of advanced defense, security, and aerospace systems. BAE Systems employs 88,200 people with operations in six home countries - Australia, Saudi Arabia, South Africa, Sweden, UK, US, and customers in over 100 countries.

BAE Systems, Inc., with greater than 40,000 employees, is the US subsidiary of BAE Systems plc. The US focus is:

- Support and service solutions for current and future defense, intelligence, and civilian systems.
- Design, develop and manufacture a wide range of electronic systems and subsystems for both military and commercial applications;
- Design, develop, produce, and provide service support of armored combat vehicles, artillery systems and intelligent munitions.

Site Overview:

BAE Systems in Manassas, VA offers advanced systems and components for missions such as space control; intelligence, surveillance, and reconnaissance; environmental and space science; communications; and navigation. This includes notable programs like the computers for the Mars rovers. The Manassas site is a complete design, packaging, and test facility for development and production of CMOS microelectronic technology and other novel devices.

Intern Responsibilities:

BAE Systems Manassas is looking for summer interns to work in integrated circuit modeling, design, simulation and test. Job responsibilities include hands on circuit design and test. Interns develop skills to use design and modeling software, to develop and test a host of digital devices such as advanced microprocessors, memories, ASICs and other high function devices.

Requirements:

We are interested in students completing their sophomore or junior year in electrical engineering with a desire to grow and learn about microelectronics. Students attending Virginia Tech, University of Virginia, Old Dominion University, Virginia Commonwealth University, The College of William and Mary, and George Mason University may apply.

BAE Systems is committed to a high performance culture and provides an environment that challenges our employees to be remarkable and obtain their full potential. We are an EEO/Affirmative Action Employer that understands the value of diversity and its impact on a high performance culture.

Micron Technology, Inc. (Manassas, Virginia)

Company Overview:
For more than 30 years, Micron's teams of dreamers, visionaries, and scientists have redefined innovation—designing and building some of the world's most advanced memory and semiconductor technologies. We develop the technologies that transform what's possible. In fact, you likely use our memory every day—in products from computing, networking, and server applications, to mobile, embedded, consumer, automotive, and industrial designs.

As one of the most prolific patent holders in the world we continually rethink, recast, and advance new ideas to bring innovation to broader markets and find ways our technology can inspire new applications or make fundamental improvements to existing designs.

Our roots are in memory, the core strength of our business. As we look toward the future, we'll continue to build on our past achievements by leveraging the synergies between our core memory business and diversified products and technologies that help drive innovation and growth in new markets.

Site Overview:
Micron Technology Virginia manufactures memory chips used in cell phones, mobile music and video players, notebook computers and more. This site is a premier 300mm wafer fabrication facility deploying the world's most advanced memory technology.

As a leading high-tech manufacturing company in Northern Virginia we realize a strong and healthy community is critical to the success of individuals, companies and society. The Virginia site works closely with government and community organizations to improve the region's quality of life and support initiatives that positively impact the area of greater Manassas, the Prince William region and the Commonwealth of Virginia.

Responsibilities:
Challenge yourself intellectually by working side-by-side, gaining real-world experience from leading industry professionals. You will directly play a pivotal role in continuing the aggressive growth of one of the world's leading providers of advanced semiconductor solutions. During your internship you will work on projects in the areas of product characterization and yield analysis, new tool implementation and process enhancement and new product implementation.

Requirements:
Currently attending one of the following Institutions:

- Virginia Polytechnic Institute, University of Virginia, Old Dominion University, George Mason University, The College of William and Mary, Virginia Commonwealth University, Virginia Military Institute

Current Junior or Senior pursuing a BS in any of the following disciplines:

- Microelectronic Engineering, Electrical Engineering, Chemical Engineering, Materials Science, Computer Engineering

Projects for 2019 VMEC Summer Scholar

George Mason University

The VMEC summer scholar can select one of the following projects:

Project 1: Infrared sensor network

This project is to design and build an intrusion detection and positioning system based on an infrared sensor network. The infrared sensor network consists of infrared (temperature) sensors, wireless antenna modules and data analysis units. The system will be used to differentiate targets with different temperatures and target location. Data analysis method will be developed to calculate target position and speed and predict their future position at real-time.

Project 2: Precise positioning system with GPS and radio-frequency signals

The goal of this project is to develop a precise positioning and protection system for pedestrians and bicyclists. A Wi-Fi network assisted with GPS modules will be developed to detect and locate the moving pedestrians and bicyclists in the transportation. The detection precision will be significantly enhanced by using Received Signal Strength Indicator (RSSI) method. The real-time position and speed of the moving targets will be measured and analyzed. The results will be transferred to a monitoring server used for transportation safety purpose.

Mentor: Dr. Qiliang Li, Dept. of Electrical and Computer Engineering, VMEC Professor, George Mason University, Fairfax, VA. Tel: (703) 993-1596; e-mail: qli6@gmu.edu

VMEC SUMMER SCHOLAR INTERNSHIP

WILLIAM & MARY

Project Title: Microwave near-fields for atom chips and ultra-cold atoms.

The objective of this project is to develop tools for generating and probing atom chip-based near-fields at RF and microwave frequencies. Atom chips are used for trapping and cooling ultra-cold atoms (10 nK – 100 μK) to engineer quantum sensors.

Atom chips, have been used extensively for trapping atoms with static magnetic fields generated from DC currents, but the use of microwave near-fields for trapping has only begun to be explored. Importantly, microwave fields offer the possibility of producing spin-dependent potentials for coherent manipulation of quantum gases such as Bose-Einstein condensates. This capability is important for quantum information processing and matter-wave interferometry.

The VMEC candidate should have some knowledge of RF and microwave engineering, EM simulation, and lasers, and an interest in quantum physics.

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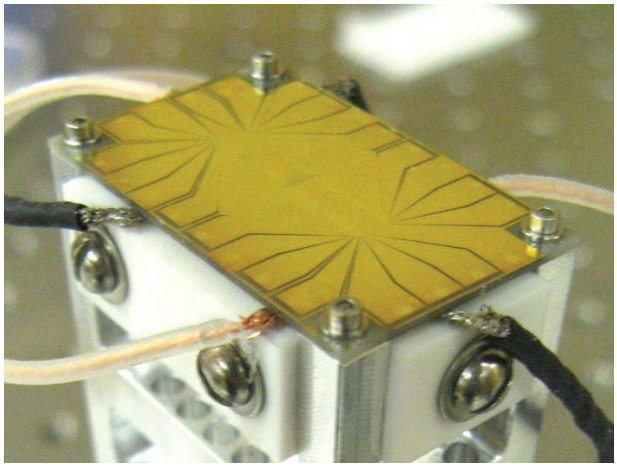


Virginia Commonwealth University

Wright-Virginia Microelectronics Center at VCU

Virginia Commonwealth University (Richmond, VA) hosts 8000 ft^2 of state-of-the-art, class-100 cleanroom laboratories in its Wright-Virginia Microelectronics Center. The VCU VMEC Internship offers the unique opportunity to work independently in this high-tech facility and really "do it yourself". You will have the opportunity to work hands-on, from initial concept to final testing and obtain a complete microfabrication experience, including:

(1) CAD layout and design of a microelectronic device,
(2) Photomask fabrication using our own custom maskmaking facilities,
(3) Device fabrication in the W-VMC clean room and
(4) Device testing in our characterization lab.

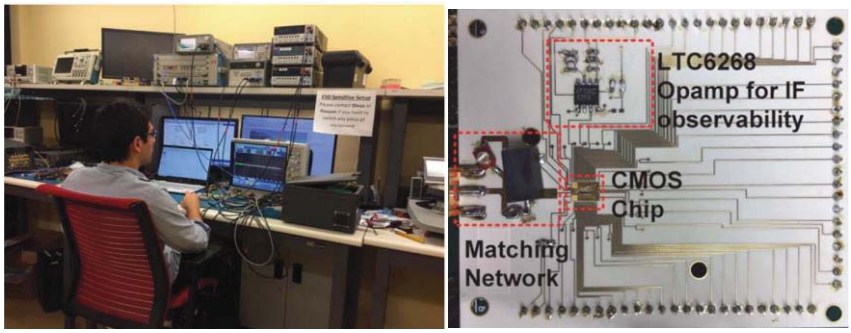
Training will also include standard clean room protocol and safety training. The technology for this fabrication project will vary, and in the past has included MOSFETS, Polymer Based Micromachines, surface acoustic wave (SAW) devices and solar cells.

University of Virginia

Project 1: Ultra-Low-Power Wireless Sensor Node Links

Integrated Electromagnetics, Circuits and Systems Lab – mentor: prof. Steve Bowers
https://engineering.virginia.edu/faculty/steven-m-bowers

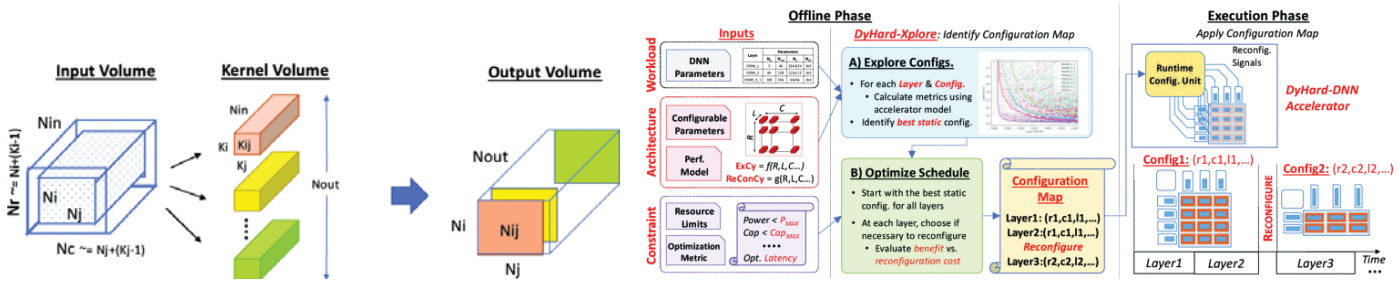
This project will build off of nano-watt level radios previously developed in the Integrated Electromagnetics, Circuits and Systems lab to implement demonstrations of wireless sensor node links, to develop a wireless sensor link for smart city and Internet of Things (IoT) applications. Investigations of mobile phone to node, and node to node communication will be made, with a goal of demonstrating a node that can operate using energy harvesting, can be woken up by a mobile phone to take a measurement, and to deliver that data back to the phone. A background in Electronics/Electronics 2 is important, and an RF circuits or microwave engineering class will enable more advanced topics to be explored. The figure below show the measurement setup and PCB for Nanowatt level wake-up receiver designed by a previous summer scholar.



Project 2: DyHard-DNN: Deep Neural Network Acceleration with Dynamic Hardware Reconfiguration

High Performance Low Power (HPLP) Lab - http://hplp.ece.virginia.edu/ – mentor: prof. Mircea Stan
https://engineering.virginia.edu/faculty/mircea-r-stan

Deep Neural Networks (DNNs) with static hardware parameters run sub-optimally and leave energy-efficiency margins unclaimed. This project will investigate DyHard-DNNs, where accelerator microarchitectural parameters are dynamically reconfigured during DNN execution to significantly improve metrics of interest. The key idea of DyHard-DNNs is to reconfigure the microarchitectural parameters of the accelerator dynamically, based on the characteristics of the layer under execution. The costs of augmenting the accelerator with the ability to reconfigure depends on the implementation scenario. For the case of ASIC design, under an iso-power constraint, reconfiguration involves clock/power-gating computation slices or interconnect links based on DNN layer dimensions. In contrast, reconfiguration in FPGA designs involves loading a new full or partial bitstream. A background in basic Digital Design and/or basic Programming is important, while a more advanced FPGA or VLSI design class will allow more advanced topics to be explored. The figure below illustrates the design space for DNN that is being considered in the HPLP lab.



Old Dominion University

Applied Research Center at Thomas Jefferson National Accelerator Facility Newport News, VA

Project Title: "Physical Characterization and Electrical Measurements of high-k Dielectric Films deposited by Atomic Layer Deposition (ALD) "

This research project involves the growth of high-k dielectric films by Atomic Layer Deposition (ALD) for advanced gate stack engineering. Examples of the ALD films which will be studied are HfO_2, Al_3O_2, ZrO_2, TiO_2 and includes semiconducting ZnO films. These novel electronic materials will replace the conventional SiO_2 gate dielectric of MOS Field Effect Transistors in the future beyond the 45 nm technology node. These high-k dielectric films will be grown with suitable chemical precursors and need to be post deposition annealed by Rapid Thermal Annealing (RTA). The physical characterization will be performed with spectroscopic ellipsometry, Atomic Force Microscopy (AFM), optical microscopy and scanning and transmission electron microscopy (SEM & TEM). X-ray Diffraction (XRD), SIMS etc. The electrical measurements will include I-V and C-V measurements of MOS Capacitors. The overall project also includes photo lithography of suitable capacitor structures, ALD film deposition technique, and various post-deposition RTA annealing cycles. For the film deposition by ALD, surface treatment such as nitridation can also be introduced. Our ALD projects include work with porous alumina membranes, which are coated or filled with ALD ZnO to fabricate novel ZnO nano-tubes or nano-rods for sensor and detector applications. This VMEC summer project will provide a unique opportunity for undergraduate students to receive hands-on laboratory training in state-of-the-art thin film Atomic Layer Deposition (ALD) technology, which will play a crucial role for the deep nano-technology node of future CMOS device generations.

Advisor: Dr. Helmut Baumgart, VMEC Professor, Department of Electrical and Computer Engineering ,Old Dominion University

VMEC Summer Scholar

Virginia Tech

1. Fabrication and evaluation of Si and Ge Nanomembranes, Nanoribbons and Nanowires.

A process flow has been developed at Virginia Tech to manufacture nanomembrane, nanoribbon and nanowire strucures using SOI-type wafers and standard CMOS manufacturing techniques. The goal of the project is to investigate the properties of lower dimensional systems in terms of resistivity, carrier mobility, diffusion and interface effects. The project requires participation in CMOS process technology such as lithography, layer deposition by Chemical Vapor Deposition (CVD), Reactive Ion Etching (RIE), wet etching, metallization. The student will also participate in characterization of the structures in terms of mobility chemical composition (SIMS), resistance, carrier density, and temperature effects.

2. **Metal Ion Transport in Solid Electrolytes and the Formation of Nanowire Bridge Switches**

We are investigating the formation of nano-metal bridge formation in electrolytes between two metalic electrodes. The formation of the metal nanofilement is being used as a basic mechanism for a new type of non-volatile memory, caleld resistive RAM or RRAM. The student will be involved in manufacturing of such structures using Physical Vapor Deposition (PVD) and Atomic Layer Deposition (ALD). He or she will be using lithography to define the basic cross-bar structure. The student will participate in the evaluation of the memory function of such a device. Some priopr experience with clean room technology is desired but not necessary.

The project - a collaboration between Virginia Tech (VTech), National Institute of Standards (NIST), and Old Dominion University - aims to elucidate the atomistic mechanisms of the metal ion migration and filament formation and its disconnection. It is the objective of the present study to ascertain the responsible mechanisms for: i) injection of Cu ions from electrode into the electrolytes, ii) drift-diffusion-reaction mechanisms for Cu ions transport, trapping, clustering, and agglomeration, iii) the dependence of the transport mechanisms on temperature, stress, and the strength of the atomic bonds, iv) statistical distributions for filament formation and its dismantlement. v) The factors that control the quality of the filament.

Contact:
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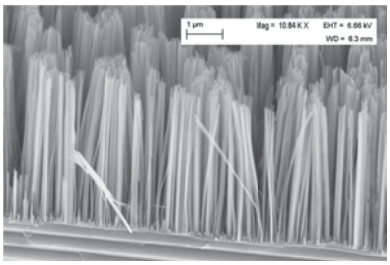
2019 VMEC Summer Scholar

Norfolk State University

1. Fabrication of Silicon Nanowire Arrays for Reducing Surface Reflection

Silicon nanowire (SiNW) arrays are useful to reduce surface reflection of silicon substrates significantly below its 35% reflectivity. The reduction in reflectivity should lead to enhanced performance of silicon detectors, solar cells and other optoelectronic devices. This project will investigate the antireflection properties of SiNW and any resultant enhancement in quantum efficiency of such devices.

The student will fabricate SiNW using Ag assisted catalytic etching method that is simple and does not require expensive equipment to fabricate large area samples. A high degree of control on the diameter, length, and density of SiNW can be achieved using the AgNO3/HF solution that provides the Ag nanoparticles for catalytic etching. The VMEC summer project will focus on the following topics:

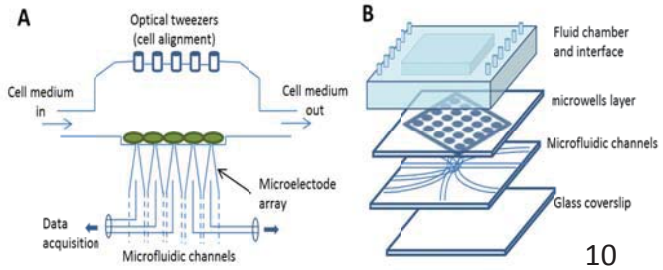


1. Metal assisted etching of Si surface to produce SiNW.
2. Surface reflectivity of the nanostructured silicon surface.
3. Effect of low reflectivity of nanostructured silicon surface of a Si p-n junction.

NSU has excellent cleanroom facilities to conduct the chemical fabrication. The surface structures will be studied using high resolution scanning electron microscopes and atomic force microscopes. Reflectivity will be measured using integrating sphere and spectrometer. Si p-n junctions will be fabricated using diffusion and/or ion implantation and annealing. Quantum efficiency will be measured using our solar cell research facility.

2. Design and Fabrication of optofluidic chip for biological electrophysiology measurements

Excitable biological cells exhibit mechano-electric sensitivity by which their electrical behavior is modulated by mechanical stimuli or stretch. Specialized stretch-activated ion channels in cells are thought to be responsible for this mechano-electric modulation. The goal of this project is to design a microfluidic-based platform to record electrophysiological currents from biological cells in their stretched conditions. A microfluidic chamber consisting of an array of micro-wells will be designed as depicted in the schematic below. Each microwell will be equipped with a microelectrode recording assembly underneath the substrate. The cells will be trapped and guided to the microwells using computer-controlled optical tweezers. A novel optical non-contact cell stretching method using counter-propagating laser beams, carried to the microwells via optical waveguides, will be designed to produce a controlled stretch in the trapped cells. The proposed optofluidic chip will be used to systematically characterize the stretch-activated ion channels in biological cells. The proposed research has potential to provide mechanistic breakthroughs in our understanding of several chronic diseases such as heart failure and hypertension.



Contact:
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Department of Engineering
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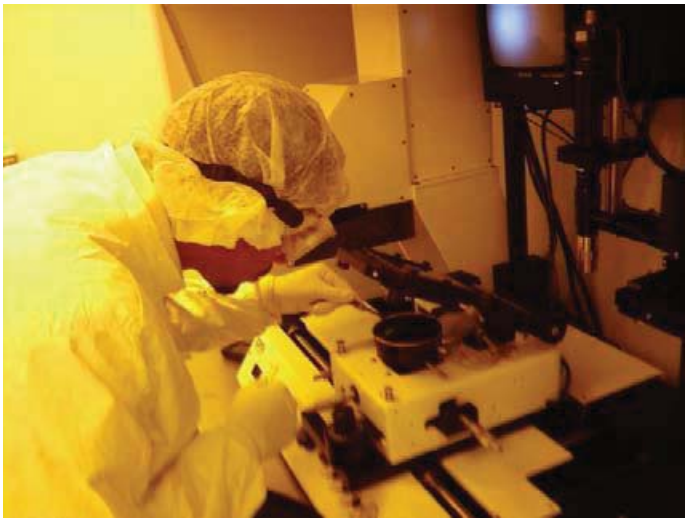
The student will work in a team with other graduate students and faculty involved in the project. The student will get an opportunity to use the modern cleanroom facility in the Department of Engineering, and learn experimental techniques and algorithm development in Matlab and C++.



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